NP

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,949	10/26/2001	Makoto Yamamoto	44471-265522 (13700)	3657

23370 7590 03/20/2002

JOHN S. PRATT, ESQ
KILPATRICK STOCKTON, LLP
1100 PEACHTREE STREET
SUITE 2800
ATLANTA, GA 30309

EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 03/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/014,949	YAMAMOTO ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *14-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C.119 (a)-(d), claiming priority from Japanese Patent Application No. P 2001-128187 filed April 25, 2001 which papers have been placed of record in the file.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-13 are, drawn to a transistor and the transistor in a integrated circuit, classified in class 257, subclass 500.

II. Claims 14 –19 are, drawn to a method of making a transistor in a semiconductor integrated circuit , classified in class 438, subclass 358.

Inventions Group I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process, namely instead of growing an epitaxial layer depositing an semiconductor layer of second conductivity on the first diffusion region.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Roger T. Frost , (Reg. No. 22,176) Esq. on March 12, 2002 (4.35p.m.) at (404) 815-6500 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-13.

Affirmation of this election must be made by applicant in replying to this Office action.

Claims 14-19 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 112

I. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

II. Claims 2 - 3 and 10-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 2 and 10 the phrase "the second electrode region surrounds said graded base region" renders the claim indefinite because the term "the second electrode region surrounds said graded base region" is characterized according to applicant's own definition merely means the second main electrode (or the first collector region) as shown in figure 2 C and # 7 shows the region 7 not surrounding the region 5 but placed on either side of it; if applicant desires to recite the position of

the second main electrode with respect to the graded base, Applicants' may recite that " wherein the second main electrodes are placed on either side of the graded base ".

Claims 3 and 11 are rejected at least for depending upon rejected claims 2 and 10.

Further the claims are a literal translation from a foreign language and need to be corrected for correct English grammar eg. are

Claims 5,8 and 13 line 2 "wiring contacting with "

Claims 3,11 line 2 "rectangular ring shape "

Applicants' cooperation is sought to correct the errors .

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-13 are rejected under 35 U.S.C.102(b) as being anticipated by unpatentable over Bergeron et al. (U.S. Patent No. 4,326,212, herein after Bergeron).

With respect to claim 1, Bergeron describes a lateral transistor including :.

a semiconductor substrate of the first conductivity type (Bergeron, fig.1 D # 2, col. 4 line 32 , vertical NPN with N base substrate and lateral PNP with P base substrate col. 3 line 57,col. 3 lines 4-5) , a buried region of the second conductivity type

disposed on said semiconductor substrate (Bergeron fig.1d # 6, col. 3 lines 31-N-type), a uniform base region of the second conductivity type disposed on the first buried region (Bergeron fig.1e # 36 and 40, col. 4 lines 58- N-type), a plug region of second conductivity type disposed in said uniform base region, the plug region protrudes from a top surface of the uniform base region so as to reach to the buried region (Bergeron fig.1e # 32, col. 4 lines 43-N type), first and second main electrode regions of the first conductivity type disposed in and at the top surface of the uniform base region. (Bergeron fig.1h # 54, 60, 62 col. 5 lines 17- P type), a graded base region of the second conductivity type disposed in the uniform base region, enclosing bottom and side of the first main electrode region, the graded base region has a doping profile such that the impurity concentration decreases towards the second main electrode region from the first main electrode region (Bergeron fig.1j, col. 5 lines 25-35), wherein the combination of the uniform base region and the graded base region serve as a base region (Bergeron fig.1j # 40 and 74, col. 5 lines 52-57).

With respect to claims 2 and 3, to the extent understood, wherein the second main electrode is ring, rectangular shaped and surrounds the graded region regions (Bergeron figures 1a - 1 j 54, 62 etc. as shown in are identical to those shown in figs. 2c-d, 3 m-p of the instant application and further surround graded base region 74).

With respect to claim 4, wherein the base contact region is disposed in and at a top of the plug region (fig.1 h –j # 70 in and at a top of 36).

With respect to claim 5, a base wiring contacting with base contact region (It is inherent that the base contact region has to be in electrical contact with a base wiring in order to function as a base contact).

With respect to claim 6, wherein the semiconductor integrated circuit having lateral transistor includes :

An integrated circuit (Bergeron fig. 1, col. 1 line 15having a semiconductor substrate of the first conductivity type (Bergeron, fig.1 D # 2, col. 4 line 32 vertical NPN with N base substrate and lateral PNP with P base substrate col. 3 line 57,col. 3 lines 4-5) , a buried region of the second conductivity type disposed on said semiconductor substrate (Bergeron fig.1d # 6, col. 3 lines 31-N-type), a uniform base region of the second conductivity type disposed on the first buried region (Bergeron fig.1e # 36 and 40, col. 4 lines 58- N-type), a plug region of second conductivity type disposed in said uniform base region, the plug region protrudes from a top surface of the uniform base region so as to reach to the buried region (Bergeron fig.1e # 32, col. 4 lines 43-N type), first and second main electrode regions of the first conductivity type disposed in and at the top surface of the uniform base region. (Bergeron fig.1h # 54, 60, 62 col. 5 lines 17-P type), a graded base region of the second conductivity type disposed in the uniform base region, enclosing bottom and side of the first main electrode region, the graded base region has a doping profile such that the impurity concentration decreases towards the second main electrode region from the first main electrode region (Begeron fig.1j, col. 5 lines 25-35), wherein the combination of the uniform base region and the graded

base region serve as a first base region of the lateral transistor (Begeron fig.1j # 40 , col. 4 lines 58).

With respect to claim 7, wherein the second buried region of the second conductivity type disposed on the semiconductor substrate and forming a part of the third main electrode region of the VFET (Fig. 1h # 54 forming collector (electrode) of NPN transistor (Vertical transistor col. 5 line 13) , a drift region of second conductivity type disposed on the second buried region (Fig. 1a –j # 4, col. 4 line 32), a second base region of first conductivity type .disposed in the drift region (fig. 1 a-j # 36 in region 4), a fourth main electrode region of second conductivity type disposed in the second base region (fig. 1 a-j # 70, col. 5 line 14).

With respect to claim 8, a second base wiring contacting with second base contact region (It is inherent that the base contact region has to be in electrical contact with a base wiring in order to function as a base contact).

With respect to claims 10 and 11, to the extent understood wherein the second main electrode is formed in a ring shape (Bergeron figures 1a - 1 j 54,70 etc. as shown in are identical to those shown in figs. 2c-d, 3 m-p of the instant application col.3 line 4, col.3 line 7 and further surround graded base region 74).

With respect to claim 12, wherein a first base contact region is disposed in and at the top surface of the plug region . (fig.1 h –j # 62 in and at a top of 36)

With respect to claim 13, wherein the first base wiring is in contact with the first base region. (It is inherent that the base contact region has to be in electrical contact with a base wiring in order to function as a base contact).

With respect to claim 9, wherein an element isolation region is disposed between the uniform base region and the drift region (Bergeron fig. 1j # 42 between 36 and 4 and isolating them, col. 4 line 55)

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7722.

Steven H. Rao

Patent Examiner

March 15, 2002.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800